Activities at Univ. Barcelona

Ll. Garrido Barcelona, 29 April 03



- Starting: 96
 - in collaboration with IFAE we join the HERA-B experiment
 - Main activity: RICH
- On 98
 - we join the LHCb collaboration
 - Main activity: The SPD chamber of the calorimeters

IERA-B



test of the ASD8 electronics (start of the electronics lab.)
maintenance and operation of the RICH
reconstruction program (PID)
data analysis (3 Ph.D.)

No additional effort on this experiment any longer

HCb



Discriminate neutral/charged at level-0 trigger





HCb

responsibilities





- Farm with 20 PC's
- LHCb MC generation





IP: Ricardo Graciani





Very important collaboration from the electronics department of our faculty of physics and from the University Ramon Lull

People		
ECM (UB)	Elect. (UB)	Elect. (URL)
R. Graciani	S. Bota	X. Vilasis
D. Gascon	A. Dieguez	J.Riera
E. Aguilo	A. Herms	M. Rosello
M. Calvo	X. Cano	S.Luengo
S. Gomez (URV)		R. Ballabriga
E. Grauges		X. Xirgu
E. Benedico		O.Motto
Ll. G.		
•ASIC + Digital Control : U	Β	
•VFE and Control boards : U	JRL	
•PMT : UB + URL		
•PHYSICS : UB		

The role of the SPD at the Level-0 trigger



PMT test



Test

- •Absolute gain of all channels
- •Linearity test
- •Short term stability
- •Dark current

Test on reduced numbers:

Quantum efficiencyOptical CrosstalkLong term stabilityTemperature and magnetic field dependence

<image>



imulations

•Simulation of PAD's photons arrival time distribution at the PMT and its inclusion in the LHCb detector simulation, and its comparison with **cosmic ray test**:



lectronics



SIC

- •0.8 μm AMS BiCMOS Technology•Dual channel
- •Fully differential
- •SEU and SEL protection
 - Triple voting
 - Guard rings





tatus of the electronics

ASIC:

- **RUN 4** (June 2002)
- •Complete processing channel
- •separate blocs + digital ctrl
- •Works at 3.3 V to reduce power consumption
- Higher gain to meet PMT DC current limit requirements.
- **RUN 5** (July 2003)
- •8 full channels
- •Final design Prototype

•VFE

- •Prototypes working (1-4 channels)
- •End this year: 16 full channel (2 ASIC) and digital control (6-layer board)

Control Board

•Under design (1 Control Boards every 4 VFE Boards)



'owards the massive ASIC, boards and PMT test

